WHAT IS CLAIMED IS:

1. A semiconductor chip comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level; and

a boundary layer located at the boundary between the bulk device region and the SOI device region.

2. The semiconductor chip according to claim 1, wherein the bulk growth layer is a silicon bulk growth layer, and the boundary layer reaches the base substrate and is made of one of polysilicon or silicon-based compound semiconductors.

3. The semiconductor chip according to claim 1, wherein the bulk device region includes a first isolation separating the bulk device, and the SOI device region includes a second isolation separating the SOI device, the first and second isolations being of substantially the same depth.

4. The semiconductor chip according to claim 3, wherein the first and second isolations have a depth reaching the buried insulator.

5. The semiconductor chip according to claim 4, wherein the bulk device region has a pn junction positioned above the interface between the base substrate and the bulk growth

layer.

6. The semiconductor chip according to claim 1, further comprising a first isolation in the bulk device region, a second isolation in the SOI device region, and a third isolation positioned at the boundary and functioning as the boundary layer, the first, second, and third isolations being of substantially the same depth.

7. The semiconductor chip according to claim 6, wherein the first, second, and third insulators are deeper than the buried insulator.

8. The semiconductor chip according to claim 7, wherein the third insulator has a sidewall that is in contact with the buried insulator.

9. The semiconductor chip according to claim 7, wherein the bulk device region has a pn junction positioned below the interface between the base substrate and the bulk growth layer.

10. The semiconductor chip according to claim 1, further comprising a first isolation in the bulk device region, a second isolation in the SOI device region, and a third isolation positioned at the boundary and functioning as the boundary layer, the second isolation being shallower than the third isolation.

11. The semiconductor chip according to claim 1, further comprising a first isolation in the bulk device region, and a second isolation that is shallower than the first isolation, wherein the boundary layer is whichever the first or the second isolation that is positioned closest to the boundary.

12. The semiconductor chip according to claim 11, wherein the second isolation functions as the boundary layer, and has a bottom face that is in contact with the buried oxide.

13. The semiconductor chip according to claim 1, further comprising a dummy pattern in the bulk device region near the boundary.

14. The semiconductor chip according to claim 13, wherein the bulk device positioned in the bulk device region includes a DRAM cell having a trench capacitor, and the dummy pattern is a dummy capacitor.

15. The semiconductor chip according to claim 1, wherein the bulk device positioned in the bulk device region includes a DRAM cell having a trench capacitor, the trench capacitor comprising a first part extending at and below the interface between the base substrate and the bulk growth layer, and a second part extending above the interface, the width of the first part being greater than that of the second part.

16. A method for fabricating a semiconductor chip comprising:

preparing an SOI substrate consisting of a base substrate, a buried insulator on the base substrate, and a silicon layer on the insulator;

removing the silicon layer and a portion of the buried insulator in a predetermined area of the SOI substrate;

forming a sidewall protection film covering a side face of the silicon layer revealed by the removal;

exposing the base substrate in said predetermined area;

forming a bulk growth layer from the exposed surface of the base substrate until the top face of the bulk growth layer is in alignment with the top face of the silicon layer;

forming isolations having the same depth in the bulk growth layer and in the SOI substrate in a same process; and

fabricating devices in the bulk growth layer and the silicon layer on the buried insulator.

17. The method according to claim 16, wherein the base substrate is exposed by wet etching.

18. The method according to claim 16, further comprising:

removing the sidewall protection film after the formation of the bulk growth layer, wherein the fabrication of devices includes forming a gate and filling a recess resulting from the removal of the sidewall protection film with a semiconductor gate material.

19. The method according to claim 18, wherein the semiconductor gate material includes polycilicon and silicon-based compound semiconductors.

20. The method according to claim 16, wherein the formation of isolations includes providing isolation at the boundary between the bulk growth layer and the SOI substrate, while removing the sidewall protection film.

21. A method for fabricating a semiconductor chip comprising:

preparing an SOI substrate consisting of a base substrate, a buried insulator on the base substrate, and a silicon layer on the insulator;

removing the silicon layer at a first position of the SOI substrate to form a first isolation in the removed portion, a side face of the silicon layer being covered with the first isolation;

exposing a top face of the base substrate at a second position, while keeping the side face of the silicon layer covered with the first isolation;

forming a bulk growth layer from the exposed surface of the base substrate until the top face of the bulk growth layer is in alignment with the top face of the silicon layer;

forming a second isolation in the bulk growth layer, the second isolation being deeper than the first isolation; and

fabricating devices in the bulk growth layer and the silicon layer on the buried insulator.

22. The method according to claim 21, wherein the formation of the first isolation includes providing an isolation at a position that is to be a boundary between the bulk growth layer and the SOI substrate.

23. The method according to claim 21, wherein the formation of the first isolation includes providing an isolation to the sec.0ond position at which the base substrate is to be exposed.

24. The method according to claim 21, further comprising:

forming a first part of a trench capacitor in the exposed surface of the base substrate before the bulk growth layer is formed, the first part having a first width; and

forming a second part of the trench capacitor in the bulk growth layer, the second part being connected to the first part and having a second width narrower than that of the first part.

25. A method for fabricating a semiconductor chip comprising:

preparing an SOI substrate consisting of a base substrate, a buried insulator on the base substrate, and a silicon layer on the insulator;

removing the silicon layer and the buried oxide in a predetermined area of the SOI substrate to expose the base substrate;

forming a first part of a trench capacitor in the exposed base substrate;

forming a bulk growth layer on the exposed base substrate until the top face of the bulk growth layer is in alignment with the top face of the silicon layer on the buried insulator; and

forming a second part of the trench capacitor connected to the first part and having a second width narrower than the first width.

26. The method according to claim 25, further comprising:

forming isolations in the bulk growth layer and in the SOI substrate in the same

process.

27. A method for fabricating a semiconductor chip comprising:

preparing an SOI substrate consisting of a base substrate, a buried insulator on the base substrate, and a silicon layer on the insulator;

removing the silicon layer and the buried oxide in a predetermined area of the SOI substrate to expose the base substrate;

forming a bulk growth layer on the exposed base substrate until the top face of the bulk growth layer is in alignment with the top face of the silicon layer on the buried insulator;

forming a dummy pattern in the bulk growth layer near the boundary with the SOI substrate, the dummy pattern being deeper than the buried insulator; and

fabricating devices in the bulk growth layer and in the SOI substrate.

28. The method according to claim 27, wherein the formation of the dummy pattern includes forming a trench capacitor in the bulk growth layer in the same process as for forming the dummy pattern.